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ascatron

SiC EPITAXY SERVICE

Complete range of SiC Epitaxy

- From R&D epi material to prototype development and pre-volume production
- Flexible specification
- Multi-layer structures
- Epitaxially grown pn-junctions
- Support device design

Key Parameters	
Wafer size	76, 100, 150 mm
Polytype	4H, 6H, 3C
n-doping	$10^{14} – 10^{19}$ cm^{-3}
p-doping	$10^{14} – 10^{20}$ cm^{-3}
V-doping	semi-insulating
Ge-doping	resistivity control
Thickness	0.1 - 250 µm

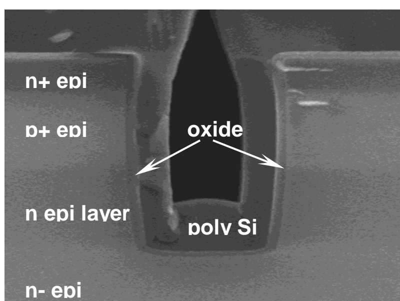
SiC Epitaxy Equipment

Single wafer epitaxy	LPE PE106, Aixtron VP508
Multi wafer epitaxy *	Aixtron VP2400
Surface polishing *	Surface grinding, back-grinding, polishing and CMP
Characterization *	FTIR, CV, Microscope, Candela defect mapping, AFM, SEM

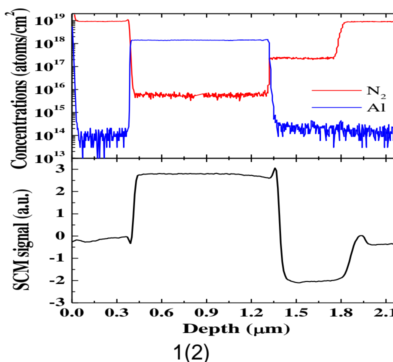
* Available through cooperation with NORSTEL, Sweden

3DSiC®: In process & regrowth epitaxy, multi-layer structures

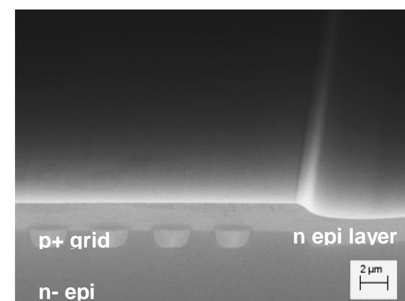
Trench MOSFET



Multi-Layer



Buried Grid



State of the art SiC epitaxy technology

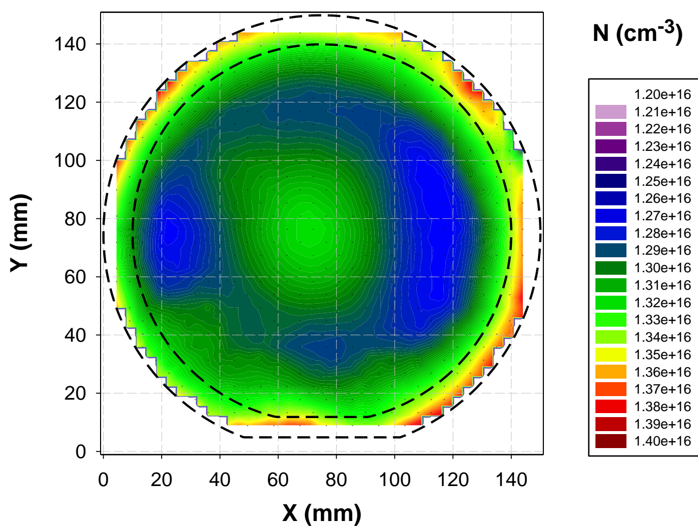
250µm thick layer
1 downfall, 1 triangle, 1 carrot defect
$\Rightarrow$ 0.012 defects / cm^2

Record low defect density through efficient buffer layer technology

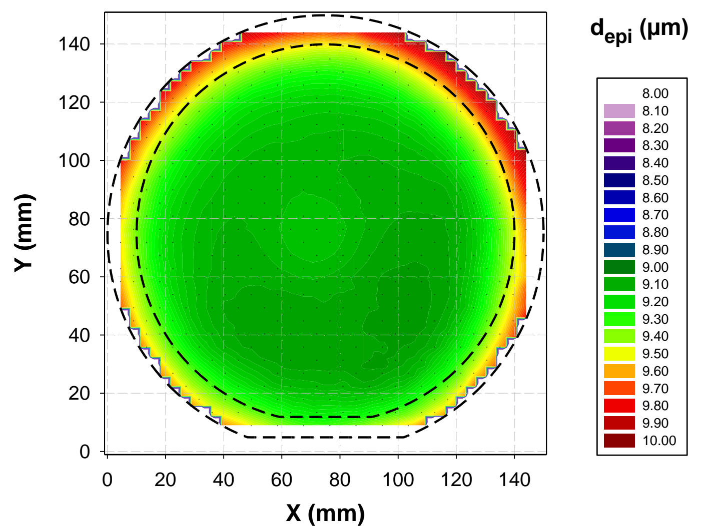
- Prevent nucleation of crystalline defects at growth start
- BPD to TED conversion rate > 99.8%
  ⇨ < 1 BPD per cm^2
- Enables bipolar SiC device technology

Best in class layer homogeneity with LPE PE106

- Adjustable lateral gas flows
- High Growth rate of 40µm/h using TCS as silicon precursor
- Thick layer growth up to 250µm thickness and more
- Low doping concentrations of ~$1 \cdot 10^{14}$/cm^3
- Enables >15kV SiC device technology



	150 mm diameter	140 mm diameter	130 mm diameter
#points	408	371	320
MEAN N (cm-3)	1.31E+16	1.30E+16	1.30E+16
StdDev/Mean (%)	2.0	1.8	1.4



	150 mm diameter	140 mm diameter	130 mm diameter
#points	408	371	320
MEAN d epi (µm)	9.23	9.19	9.15
StdDev/Mean (%)	2.1	1.7	1.1

SiC DEVICE FABRICATION

Custom Specific Design

Ascatron's SiC material and device fabrication is based on 20 years' experience from SiC technology development resulting in well-established unit process modules. A custom specific manufacturing process is designed by combining and adjusting the process modules according to the customer's specific device design. In many cases Ascatron contributes with unique process technology and design solutions to improve further the device performance. The process integration is verified and evaluated in close cooperation with the customer. This enables a cost-efficient realization of manufacturing processes.

Device Prototyping

For design verification

- **Complete 100mm process line** Prototype fabrication, pilot production
- **Full process control** Traceability, Standard unit process modules
- **Wafer level testing** Measurement & analysing, Documentation

SiC Process Modules

Ascatron has developed a unique set of key processes enabling the fabrication of advanced SiC power devices, as well as for example sensors for exhaust gases, UV detection, or pressure measurement.

- **Substrate Buffer Technology** Reducing defects penetrating from substrate into device epi
- **Advanced SiC Epitaxy** Multilayer pn-junctions, thick epilayers & embedded structures
- **Ion Implantation Doping** Hot high energy implantation and high temperature anneal
- **Deep Trench Etching** 1-20 µm with precise side-wall control for void-free re-growth
- **Gate Oxide Technology** Advanced oxide technology with in-situ-doped polysilicon gate
- **Ohmic & Schottky Contact** Wide range of metal combinations and silicide processes
- **Metallisation Process** Thick Aluminium for wire bonding
- **Edge Termination** Combined with thick passivation for HV devices

SiC Device Technologies

Ascatron offer a number of power device technologies. The process can be optimized to meet the specific requirements, e.g. packaging compatible metallization.

- **Schottky diode** For material evaluation
- **JBS diode** Both implanted and epitaxial 3DSiC concepts
- **HV-PiN diode** Epitaxial anode and pn-junction grown in one run
- **Vertical DMOSFET/UMOSFET** Advanced gate oxide technology using deposited oxides
- **Epitaxial buried grid JFET** Based on embedded epitaxial technology

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SiC production resources

Processing of 100 & 150 mm diameter SiC wafers.

Process	Type	Parameters	Tools	Cap
Epitaxy	Hot-wall CVD	n/p 4H-, 6H, 3C-SiC n-doping 10^{14}-10^{19} cm^{-3} p-doping 10^{14}-10^{20} cm^{-3} Thickness up to 250 µm	Aixtron VP508GFR Aixtron VP2400HW** LPE PE106	S B S
Doping	Ion Implanter	40-330keV - Al, B, N, P RT & 600 ºC	Danfysik 1090*	S
Furnace Process	Thermal Oxidations	Wet/Dry/N_2O (900-1250ºC)	Thermco 5200	B
	LPCVD	Polysilicon IDP	Expertech CTR-200	B
	Annealing	1400-1800 ºC in Ar	Centrotherm Activator 150	B
	RTP		Mattson 100 RTP	S
Plasma Deposition	PECVD	SiO_2, Si_3N_4	Oxford Plasmalab 80 Applied Materials P5000	S S
Plasma Etching	RIE		Oxford Plasmalab 80 Oxford Plasmalab 100 Applied Materials P5000	S S S
	ICP		STS ICP DRIE Oxford ICP380	S S
	Microwave plasma	O_2	TePla300	B
Wet Etching	Wet cleaning process	Acid and solvent based		B
Metallisation	Plasma sputter	Au, Ni, Al, Ag, TiW	KDF 844NT, MRC 643	B
	Ion-beam sputter	Au, Ni, Al, Ti	Commonwealth IBS	B
	Evaporation	Au	PAK600	B
Lithography	Contact	Alignment Accuracy ~1µm Minimum Features ~1.5µm	Karl Suss MA8	S
	Stepper	Alignment Accur. ~ 0.3 µm Minimum Features ~ 1 µm Alignment Accur. ~ 0.1 µm Minimum Features ~ 0.75 µm	ALS 2035 G-line Nikon NSR TFHi12 I-line	S B
	Lift-off			B
Metrology	SEM		Zeiss Ultra 55, Hitachi S-3400N	S S
	Ellipsometer		Horiba Uvisel ER SENTECH instrum.	S S
	Surface Profiler		Tencor-P10, Dektak3ST	S S
	AFM		Veeco Dimension 3100	S
	Sheet Resistance	4-point probe	Four Dimension 280	S
	Inspection Microscope		Nikon, Olympus, Leitz	S
Testing	Automated Probing		Karl Suss PA 150 Electroglass	S B
Dicing	High Speed Saw		Disco DFD640	S
Polishing	CMP	Removal 0.1-1.0 µm Rms < 1 nm	AVANTI/ IPEC 472	S

Capacity of respective tool is marked as single wafer (S) and batch processing (B). * Performed at Ion Technology Center, Ångström Laboratoty in Uppsala** Performed at Norstel AB in Norrköping